SYNCHRONIZING SIGNAL INVERSION CIRCUIT

Patent number: JP3196186 (A)

Publication date: 1991-08-27

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Classification:

- international: ***G09G3/36; G09G5/12; G09G5/18; H04N5/04;*** **G09G3/36; G09G5/12; G09G5/18; H04N5/04;** (IPC1-7): G09G3/36; G09G5/12; G09G5/18; H04N5/04

- european:

Application number: JP19890337123 19891226

Priority number(s): JP19890337123 19891226

Abstract of **JP 3196186 (A)**

PURPOSE:To eliminate a control terminal which instructs the signal polarity of a synchronizing signal from the outside and to automatically discriminate the signal polarity of the synchronizing signal by providing an EOR which inverts the synchronizing signal with the MSB of an up/down counter.
CONSTITUTION:The circuit is equipped with the up/down counter 11 by which up-count and down/count are switched with the signal polarity of an inputted synchronizing signal. Furthermore, it is equipped with circuits 12-14 which control the Enable terminal of the up/down counter 11 with the overflow detection signal and the underflow detection signal of the up/down counter 11, and it inverts the synchronizing signal with the MSB output signal of the up/down counter 11 by using the EOR 16. In such a way, it is possible to eliminate the control terminal which instructs the signal polarity of the synchronizing signal from the outside, and to discriminate the signal polarity of the synchronizing signal in the inside.